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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Maurizio Peri et al Attorney Docket No.: 856063.579

Application No.: 09/265,119

Filed: March 9, 1999 Examiner: A. I. Sharon

Title: EMULATED EEPROM MEMORY DEVICE AND CORRESPONDING METHOD

DECLARATION UNDER 37 C.F.R. § 1.132

TO THE COMMISSIONER FOR PATENTS:

I, **DECLARANT'S NAME**, state as follows:

A. I am currently employed by ST Microelectronics S.r.l., which is the assignee of record of the above-referenced U.S. patent application.

B. I am familiar with the structure and operation of the STMicroelectronics' ST9, including its memory architecture.

C. Prior to September 1998, the ST9 as made and sold did not make part of the Flash memory look like EEPROM by software.

D. Prior to September 1998, the ST9 as made and sold did not make part of the Flash memory look like EEPROM by hardware.

E. Prior to September 1998, the ST9 as made and sold did not contain the following described devices:

1. An emulated EEPROM memory device, comprising a memory macrocell which is embedded into an integrated circuit having a microcontroller, the memory macrocell including a Flash memory structure formed by a predetermined number of sectors, wherein at least two sectors of the Flash memory structure are structured to emulate EEPROM byte alterability.

2. A Flash memory device for emulating an EEPROM, comprising:

a) first and second Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second Flash memory portions, all of the memory locations sharing a same address being a set of memory locations;

b) a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location; and

c) a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.

F. Prior to September 1998, the ST9 as made and sold did not carry out the following described methods:

1. A method for emulating features of an EEPROM memory device incorporated into a memory macrocell which is embedded into an integrated circuit that also includes a microcontroller and a Flash memory structure formed by a predetermined number of sectors, comprising using at least two sectors of the Flash memory structure to emulate EEPROM byte alterability by dividing each of said at least two sectors into a pre-determined number of blocks of the same size and each block into a pre-determined number of pages and updating the emulated EEPROM memory portion programming different memory locations in a single bit mode, wherein at a page update selected page data are moved to a next free

block and, when an EEPROM sector is full, all the pages are swapped to another EEPROM sector.

2. A method of emulating an EEPROM using Flash memory, the method comprising:

a) dividing the Flash memory into first and second memory sectors each including a plurality of memory blocks, each memory block including plural memory pages each with plural memory locations;

b) assigning to each memory page of the first and second memory sectors a page address that is shared by a corresponding page in each of the memory blocks of the first and second memory sectors;

c) in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector; and

d) in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: _____

_____
DECLARANT'S NAME
Residence Address:
STREET ADDRESS
CITY ADDRESS

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2. A Flash memory device for emulating an EEPROM, comprising

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a) first and second Flash memory portions each including plural memory blocks with plural memory locations, each of the memory locations sharing an address with a corresponding memory location in each of the blocks of the first and second Flash memory portions, each of the memory locations sharing a same address being a set of memory locations,

b) a plurality of memory pointers each reflecting which memory block includes a current memory location for a set of memory locations, each set of memory locations including a current memory location, and

c) a memory controller structured to, in response to receiving a request to write data to a selected address assigned to a selected one of the sets of memory locations, determine from a memory pointer associated with the selected address which memory location in the selected set is a next memory location following the current memory location for the selected set and write the data in the next memory location.

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c) in response to a first write instruction to write to a selected page address, writing to a data page of a first memory block of the first memory sector; and

d) in response to a second write instruction to write data to the selected page address, writing to a data page of a second memory block of the first memory sector.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

BC
05/17/2003

Dated: 03/14/2003

Bertrand COUTU
DECLARANT'S NAME

Residence Address:
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